Claims

[c1] What is claimed is:

1.A method of making a conductive layer on a substrate, a surface of the substrate comprising a first area and a second area, the method comprising:

forming at least one conductive layer on the first area and on the second area, respectively;

forming a first dielectric layer on the surface of the substrate that covers each conductive layer;

removing portions of the first dielectric layer and portions of the conductive layer in the first area until the remaining conductive layer in the first area is of a predetermined thickness; and

removing portions of the first dielectric layer in the second area until reaching the top surface of the conductive layer.

[c2] 2.The method of claim 1 wherein the substrate is a silicon substrate.

[c3] 3.The method of claim 1 wherein the surface of the substrate further comprises at least one second dielectric layer and at least one conductor disposed in the second dielectric layer.

[c4] 4.The method of claim 3 wherein the conductor comprises a conductive plug, a metal line, a metal interconnection or a dual damascence structure conductor.

[c5] 5.The method of claim 3 wherein the material composition of the conductor comprises tungsten (W), copper (Cu), aluminum (Al), aluminum-copper-alloy or other conductive material.

[c6] 6.The method of claim 1 wherein a method for removing portions of the first dielectric layer and portions of the conductive layer in the first area comprises:

performing a first photo-etching-process to form at least one first opening down to the top surface of the conductive layer in the first dielectric layer in the first area; and

etching portions of the conductive layer underneath the first opening so the remaining conductive layer in the first area is of the predetermined thickness.

[c7] 7.The method of claim 1 wherein a deposition process is executed to form a

third dielectric layer on the surface of the substrate so as to cover the first dielectric layer and the conductive layer in the first area before removing portions of the first dielectric layer in the second area.

[c8] 8.The method of claim 7 wherein the method for removing portions of the first dielectric layer in the second area comprises:
performing a second photo-etching-process to form at least one second opening down to the top surface of the conductive layer in the third dielectric layer and the first dielectric layer in the second area.

[c9] 9.The method of claim 7 wherein the third dielectric layer is a transparent layer.

[c10] 10.The method of claim 1 wherein the thickness of the conductive layer is approximately 12k Å , and the predetermined thickness is approximately 5k Å .

[c11] 11.The method of claim 1 wherein the material composition of the conductive layer comprises tungsten (w), copper (Cu), aluminum (Al), aluminum-cooper-alloy or other conductive material.

[c12] 12.The method of claim 1 wherein the first area is a fuse area and the conductive layer in the first area is utilized as a fuse, the second area is a bonding pad area and the conductive layer in the second area is utilized as a bonding pad.

[c13] 13.The method of claim 1 wherein the first area is a core circuit area and the second area is a periphery circuit area, the conductive layers in the first area and the second area are utilized as metal lines.

[c14] 14.A method of making a fuse, the method comprising:
providing a semiconductor substrate, a surface of the semiconductor substrate defined with a first area and a second area;
forming a first dielectric layer on the surface of the semiconductor substrate;
forming at least one first conductive layer and at least one second conductive layer on the first dielectric layer in the first area and in the second area, respectively;
forming a second dielectric layer on the surface of the first dielectric layer to

cover each conductive layer;

performing a first photo-etching-process to form at least one first opening down to the top surface of the first conductive layer in the second dielectric layer in the first area;

removing portions of the first conductive layer underneath the first opening so the remaining first conductive layer is of a predetermined thickness and is utilized as the fuse;

forming a third dielectric layer on the surface of the semiconductor substrate; and

performing a second photo-etching-process to form at least one second opening down to the top surface of the second metal layer in the second dielectric layer in the second area.

[c15] 15.The method of claim 14 wherein the semiconductor substrate is a silicon substrate.

[c16] 16.The method of claim 14 wherein the surface of the semiconductor substrate further comprises at least one fourth dielectric layer and at least one conductor disposed in the fourth dielectric layer.

[c17] 17.The method of claim 16 wherein the conductor comprises a conductive plug, a metal line, a metal interconnection or a dual damascence structure conductor.

[c18] 18.The method of claim 14 wherein the first dielectric layer further comprises a plurality of conductive plugs.

[c19] 19.The method of claim 18 wherein the method for forming each conductive plug further comprises the following steps:

performing a first etching process to form a plurality of via holes in the first dielectric layer; and

forming a metal layer in the via holes, the metal layer filling the via holes.

[c20] 20.The method of claim 14 wherein each conductive layer is an aluminum layer formed by a DC magnetron sputtering process and an etching process, and the third dielectric layer is a silicon oxide layer with a thickness of approximately 1k Å .